REMARKS

Claims 1 – 8, 10, 11, 15, 16, 18 and 19 are pending. In the above-identified Office Action, the Examiner rejected Claims 10, 11, 15, 16, 18 and 19 under 35 U.S.C. § 102(b) as being anticipated by Bruce *et al.* (U.S. Patent No. 6,000,006) hereinafter 'Bruce'. Claims 1 – 8 are rejected under 35 U.S.C. § 103(a) as being obvious over Bruce in view of Tsunoda *et al.* (U.S. Publication No. 2003/0028733) hereinafter 'Tsunoda'.

By this Amendment, Claims 1 – 8 have been canceled, Claim 15 was amended for clarity and a new Claim, Claim 20, has been presented for consideration. Claim 20 has been drawn along the lines of Claim 10 in independent form.

For the reasons set forth below, the present Application is believed to be in proper form for allowance. Reconsideration allowance and passage to issue are respectfully requested.

The present invention addresses the need in the art for a system or method for reducing average access times of slow memory technologies. In accordance with the invention, a system and method are taught for storing read and/or write pointer addresses in a buffer prior to power down. This data is used to provide for a rapid recovery on a reapplication of power so that processes may be resumed at the locations at which the processes were terminated.

The invention is set forth in Claims of varying scope of which Claim 15 is illustrative. Claim 15, as amended, recites:

> 15. A digital device that comprises:
> a memory having a **buffered memory interface** with one or more read buffers; and
> a processor coupled to the memory device and configured to retrieve stored information from the memory, **said processor being programmed to cause the memory to receive a power down command before electrical power is removed** from the memory **and** the **buffered memory interface to responsively store**, in a nonvolatile memory, **one or more addresses of memory locations that have been recently accessed**. (Emphasis added.)

None of the references teach, disclose or suggest the invention as presently claimed. That is, none of the references teach, disclose or suggest a device with a processor programmed to cause a memory interface to store memory addresses that have been recently access on the issuance of a power down command.

In the above-identified Office Action, the Examiner relied on Bruce in the rejection of Claims 10, 11, 15, 16, 18 and 19 under 35 U.S.C. § 102(b) with MPCD offered as extrinsic evidence. Bruce purports to show a system for wear-leveling non-volatile flash RAM mass storage. As to Claim 15, the Examiner suggests that at column 13, lines 31 – 34, Bruce teaches the storage of recently used addresses on receipt of a power down command. However, this assertion is not supported by the reference.

That is, at best, Bruce teaches a cache indexing or remapping scheme by which addresses are stored in a backup nonvolatile memory and used after an interruption of power. However, Bruce does not provide a teaching by which a processor issues a power down command and, more importantly, causes a buffer interface to **responsively** store recently used addresses in a nonvolatile memory. Moreover, this shortcoming of Bruce is not overcome by the teaching of Tsunoda. As shown in Figure 25, on receipt of a shut-down command, Tsunoda mere dumps data in a nonvolatile area of RAM into a mirror area in a flash memory. There is no teaching to store recently used addresses in a nonvolatile memory on receipt of a power down command as presently Claimed.

As to Claim 10, note neither Bruce nor Tsunoda teach a method including the steps of detecting of a pending power down and storage, in a nonvolatile memory, a read address for data buffered in a volatile read buffer. As mentioned above, Tsunoda mere dumps data in a nonvolatile area of RAM into a mirror area in a **flash** memory.

In short, neither Bruce nor Tsunoda teach or suggest a system capable of detecting and responding to a pending power loss to enable a rapid recovery as set forth in Claims 10 and 15. Hence, Claims 10, 15 and the Claims dependent thereon should be allowable. Inasmuch as new Claim 20 tracks Claim 10, Claim 20 should be allowable as well.

Reconsideration, allowance and passage to issue are respectfully requested.

Respectfully submitted,
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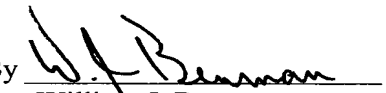
By 
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